

Customer No.: 31561  
Docket No.: 10156-US-PA  
Application No.: 10/604,692

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**REMARKS**

**Present Status of the Application**

Claims 1, 4-6, 8-10, 12 and 35-37 were rejected under 35 U.S.C. 102(b) as being anticipated by Yoshikawa (US 6,335,554) and claim 11 rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshikawa in view of Schwabe (US 4,257,832).

In response, Applicants further amended independent claims 1 and 35 and submitted the following remarks, wherein the amendment can be supported by, for example, FIGs. 1, 2A and 2B. Reconsideration of claims 1, 4-6, 8-12 and 35-37 is respectfully requested.

**Discussion of Rejections under 35 U.S.C. 102(b)**

Claims 1, 4-6, 8-10, 12 and 35-37 were rejected under 35 U.S.C. 102(b) as being anticipated by Yoshikawa.

A feature of the memory cell in amended independent claim 1 or 35 is that the split gate *as a whole* is located over the charge-trapping layer.

Yoshikawa fails to disclose the above feature. As shown in FIG. 1, a portion (8) of the split gate "3+8" is located over the charge-trapping layer 4a/b, while *another portion* (3) of the split gate "3+8" is located *beside* the charge trapping layer 4a/b *but not located over* the charge-trapping layer 4a/b.

Moreover, the above feature is not merely a trivial modification of the prior art, but is inventive over the prior art. As shown in FIGs. 2A and 2B of this invention that show the bias configurations described in claim 35 of this invention, *when a memory cell operating method of claim 35 is applied*, electrons are efficiently injected into the charge-trapping layer (104) from **both** of any two neighboring conductive pieces (130 and 140) in the programming (Fig. 2A) and the electrons in the charge-trapping layer (104) are ejected to

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**both** of the two neighboring conductive pieces (130 and 140) efficiently in the erasing (FIG. 2B), *because the split gate (130+140) as a whole is located over the charge-trapping layer (104) so that each conductive piece (130 or 140) is located over the charge-trapping layer (104) allowing electron injection therefrom and electron ejection thereto.*

On the other hand, in the operating method (FIGs. 2A-2C) proposed by Yoshikawa for the memory cell in its FIG. 1, the programming (FIG. 2A) is done by channel hot electron injection (CHEI) **but not by injecting electrons from the conductive pieces 3 and 8** and the erasing (FIG. 2B) is done by ejecting electrons to the drain **but not by ejecting electrons to the conductive pieces 3 and 8.**

Accordingly, the memory cell in this invention and that in FIG. 1 of Yoshikawa have different structures at least because they are designed for different requirements in two quite different operating methods, and the memory cell operating method of claim 35 is quite different from that disclosed in Yoshikawa.

For at least the above reasons, Applicants respectfully submit that amended claims 1 & 35 and claims 4-6, 8-10, 12 & 36-37 dependent therefrom all patently define over the prior art.

#### **Discussion of Rejections under 35 U.S.C. 103(a)**

Claim 11 were rejected over Yoshikawa in view of Schwabe. Because Yoshikawa or Schwabe fails to disclose or suggest the above feature of amended claim 1/35, claim 11 dependent from claim 1 cannot be obtained by combining Yoshikawa and Schwabe.

For at least the above reasons, Applicants respectfully submit that all pending claims including claim 11 patently define over the prior art.

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**CONCLUSION**

For at least the foregoing reasons, it is believed that the pending claims 1, 4-6, 8-12 and 35-37 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

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Respectfully submitted,

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